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EXAMINER	
NWAKAMMA, CHIBUIKE K	
ART UNIT	PAPER NUMBER
2627	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,059	PADIY ET AL.	
	Examiner	Art Unit	
	CHIBUIKE K. NWAKAMMA	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/24/2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The disclosure is objected to because of the following informalities: In the specification filed on March 24, 2008 (page 4, lines 5-6) read "one of these satellite signal is called upper satellite signals". However, the disclosure should read similar to --one of these satellite signals is called upper satellite signal--. Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 2 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 2 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 2 is drawn to a "program" *per se* or non-tangible signal with "program", per se, or non-tangible computer readable medium (as defined in the specification on page 1, paragraph [0001] as being a computer program) with "program", per se, as recited in the preamble and as such is non-statutory subject matter. See MPEP § 2106.IV.B.1.a. Data structures not claimed as embodied in tangible computer readable media are descriptive material *per se* and are not statutory because they are not capable of causing functional change in the computer. See, e.g., *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure *per se* held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between

the data structure and other claimed aspects of the invention, which permit the data structure's functionality to be realized. In contrast, a claimed tangible computer readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. Similarly, computer programs claimed as computer listings *per se*, i.e., the descriptions or expressions of the programs are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer, which permit the computer program's functionality to be realized.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 3-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanabe et al (US 2002/0034268 A1) in view of Miyanabe et al (US 6134211) and Audoin et al (US 5703845).

Regarding claim 1, Miyanabe (US 2002/0034268) discloses a cross-talk cancellation method using a main signal associated with a target track (Fig. 2, elements

S_{main}, M, MT) and satellite signals associated with side tracks (Fig. 2, elements S_{sub}, S_{sub2}, S1, S2, ST1, ST2), said main signal showing transitions and runs of various lengths between two transitions (Fig. 8 discloses multiple transitions such as [-3T,0], [-4T,0] operative on optical disk DK [0145]. Fig. 2, element DK comprises MT track associated with M beam. So, it is clear that Fig. 8 comprises main signal S_{main} and runs of various length such as [-4T,T] and [-3.5T,T]; see [0073]...DK...having plural kinds of lengths...), said cancellation method comprising the acts of:

processing said main signal (Fig. 2, element S_{dm} is a digitized version of the S_{main} and S_{main}' signal. The S_{dm} signal in inputted into the signal processing unit 6 for processing), thereby generating an improved main signal S_p, said processing including a subtraction of said filtered versions of said satellite signals from the main signal (Fig. 3, elements 6, S_{dm}, 22 and Fig. 9, elements 22,Sd_d, Sd_{d1}, Sd_{d2}, 69);

sampling said satellite signals to form sampled satellite signals with converters 8 and 10 (Fig. 2, elements S_{sub1}, S_{db1}, and S_{sub2}, S_{db2} are satellite signals that are sampled in element 6. Fig. 3, element 6 comprises sample holding circuit 18 that samples satellite signals S_{db1} and S_{db2} to form sampled signal S_e. It is obvious that S_e comprises multiple signals, i.e., signal from S_{db1} and signal from S_{db2}); and

updating coefficients of said adaptive filters by minimizing a mismatch between an actual run length [-4T,T] and an expected [-3.5T,T] run length between the two transitions of the main signal (Fig. 8; Fig. 9, elements 55-60 and [0156] comprise adaptive filters for updating means. [0183]...error that is converged to "0" during updating means read on minimizing mismatch between the actual and expected run

length between two transitions of the main signal as disclosed/admitted by applicant on page 3, lines 19-21);

filtering said satellite signals (Fig. 2, elements F1 and S_{sub1}'; F3 and S_{sub2}'), thereby generating filtered versions of said satellite signals. **However**, does not disclose converters that receive a fixed clock and adaptive filters that run on a fixed clock;; providing the improved main signal to a sample rate converter driven by a bit clock, estimating a ratio between the bit clock and the fixed clock; and taking said ratio into account during the updating act.

Miyanabe (US 6134211) discloses, converters that receive a fixed clock and adaptive filters that run on a fixed clock (Fig. 5, elements 5a-c, 10 and col. 5, lines 52-66; col. 3, lines 66-67).

providing the improved main signal SB to a sample rate converter (Fig. 5, element 400) driven by a bit clock (Fig. 5, element 10 and col. 1, lines 35-44. Note: the output of element 400 is the input to a decoding means 30. Further, element 400 is driven by the PLL circuit 10 (i.e., time recovery circuit) which generates a clock signal, i.e. bit clock. So, it is clear that element 400 equates to/ comprises sample rate converter as disclosed and/or admitted by applicant, see, page 6, lines 1-3);

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyanabe (2002/0034268) to include the teachings of Miyanabe (US 6134211) where converters are constructed to receive a fixed clock and adaptive filters that run on a fixed clock; and to update coefficients of said adaptive filters by minimizing a mismatch between an actual run length [-4T,T] and

an expected run length [-3.5T,T] between the two transitions [-3T,0], [-4T,0] of the main signal, providing the improved main signal to a sample rate converter driven by a bit clock. The modification would have been obvious for the benefit of filtering the three sequences of sampled signals on a basis of fixed predetermined coefficient, hence, producing bit synchronous samples that are needed to derive the error, i.e., mismatch, by means of calculating a difference between the extracted sample value and a reference value in order to converge to zero for updating the filter coefficient.

Miyanabe (2002/0034268) in view of Miyanabe (US 6134211) does not disclose estimating a ratio and taking said ratio into account.

Audoin discloses an estimation operator (Figs. 7a-b, element 4 and Fig. 10a, element 4; col. 6, lines 11-15) indicating a degree (claim 2, line 61; i.e., estimating a ratio) and taking said ratio into account (Fig. 10a; signals Egp, Edp comprise ratio/degree which are taking into account via elements 7-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyanabe (2002/0034268) in view of Miyanabe (US 6134211) to include the teachings of Audoin by incorporating Audoin's cross talk estimator into Miyanabe's (US 6134211) cross talk circuitry in order to estimate the ratio between the bit clock generated by Miyanabe's PLL circuit 10 and the fixed clock that is received by the A/D converters and to take into account said ratio during an updating act (col. 7, lines 60-65), so, to optimize the performance characteristics the system and to increase the bit rate of the system, hence, increase the processing speed (Audoin; Col. 1, lines 18-19 and 54-55).

Regarding claim 3, Miyanabe (US 2002/0034268) discloses a signal processor (Fig. 3, element 6) comprising cross-talk cancellation means (Fig. 3, element 22) for receiving a main signal S_{dm} associated with a target track (Fig. 2, elements MT, S_{main}, S_{main}', S_{dm}) and satellite signals S_{db1}, S_{db2} associated with side tracks (Fig. 2, elements ST1, ST2, S_{sub1}, S_{sub1}', S_{db1}, S_{sub2}, S_{sub2}', S_{db2}), said main signal showing transitions and runs of various lengths between two transitions (Fig. 8 discloses multiple transitions such as [-3T,0], [-4T,0] operative on optical disk DK [0145]. Fig. 2, element DK comprises MT track associated with M beam. So, it is clear that Fig. 8 comprises main signal S_{main} and runs of various length such as [-4T,T] and [-3.5T,T]; see [0073]...DK...having plural kinds of lengths...), said cross-talk cancellation means comprising:

updating means (Fig. 9, elements 55-60) for updating coefficients of said adaptive filters by minimizing a mismatch between an actual run length [-4T,T] and an expected [-3.5T,T] run length between the two transitions of the main signal (Fig. 8; Fig. 9 and [0156] comprise adaptive filters for updating means. [0183]...error that is converged to "0" during updating means read on minimizing mismatch between the actual and expected run length between two transitions of the main signal as disclosed/admitted by applicant on page 3, lines 19-21);

processing means (Fig. 2, element 6) for generating an improved main signal S_p from said main S_{dm} signal by subtraction of said filtered versions of the satellite signals from the main signal (Fig. 3, elements 6, S_{dm}, 22 and Fig. 9, elements 22, Sd_d, Sd_{d1}, Sd_{d2}, 69),

filtering means (Fig. 2, elements F1, F3) for filtering said satellite signals (Fig. 2, elements S_{sub1}, S_{sub2}), thereby generating filtered versions of said satellite signals (Fig. 2, elements $S_{sub1'}$, S_{sub2}', S_{db1}, S_{db2}). **However**, does not disclose filtering with adaptive filters; and time recovery means for estimating a ratio between a bit clock that drives the time recovery means and a fixed clock that drives the filtering means, and for providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients.

Miyanabe (US 6134211) discloses, converters that receive a fixed clock and adaptive filters that run on a fixed clock (Fig. 5, elements 5a-c, 10 and col. 5, lines 52-66; col. 3, lines 66-67)

time recovery means (Fig. 5, element 10. Note: applicant discloses time recovery means as a PLL circuit on page 6, line 2) and a bit clock (P signal) that drives the time recovery means 10 and a fixed clock that drives the filtering means (col. 5, lines 63-66). **However**, does not disclose, estimating a ratio and for providing said ratio to said updating means, said updating means being designed to take said ratio into account for updating said coefficients.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyanabe (2002/0034268) to include the teachings of Miyanabe (US 6134211) where converters are constructed to receive a fixed clock and adaptive filters that run on a fixed clock; and a time recovery means that is driven by a bit clock in order to estimate a ratio between the bit clock and fixed clock. The modification would have been obvious for the benefit of eliminating the amount of

time it takes for the PLL circuit to recover its synchronized state when the PLL circuit is found to be out of synchronization so to continue to reproduce data correctly (Miyanabe; Col. 3, lines 23-36).

Audoin discloses an estimation operator (Figs. 7a-b, element 4 and Fig. 10a, element 4; col. 6, lines 11-15) indicating a degree (claim 2, line 61; i.e., estimating a ratio), providing said ratio to said updating means (Fig. 10a; signals Egp, Edp comprise ratio/degree which are provided to an updating means 7-8) and taking said ratio into account for updating said coefficients (Fig. 10a and Col. 5, lines 55-58; signals Egp, Edp comprise ratio/degree which are taking into account via updating means elements 7-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyanabe (2002/0034268) in view of Miyanabe (US 6134211) to include the teachings of Audoin by incorporating Audoin's cross talk estimator into Miyanabe's (US 6134211) cross talk circuitry in order to estimate the ratio between the bit clock generated by Miyanabe's PLL circuit 10 and the fixed clock that is received by the A/D converters and to take into account said ratio during an updating act (col. 7, lines 60-65) when the ratio is provided to the updating means, so, to optimize the performance characteristics of the system and to increase the bit rate of the system, hence, increase the processing speed (Audoin; Col. 1, lines 18-19 and 54-55).

Regarding claim 6, Miyanabe (US 2002/0034268) further discloses, an apparatus (Fig. 2, element S and [0073]) for reading a signal stored along a track (ST1, MT, ST2)

on a storage medium (DK) comprising a signal processor (Fig. 2, element 6) as claimed in claim 3.

Regarding claim 4, Miyanabe (2002/0034268) in view of Miyanabe (US 6134211) and Audoin (US 5703845) discloses the signal processor as discussed in claim 3.

Miyanabe (US 2002/0034268) further discloses the signal processor as discussed in claim 3. However, does not disclose, wherein said fixed clock is asynchronous with respect to said bit clock.

Miyanabe (US 6134211) further discloses wherein said fixed clock is asynchronous (Abstract, lines 17-20) with respect to said bit clock (Fig. 6, element SYC at logic levels 1 and 0; col. 3, line 66-col. 4, line 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyanabe (US 2002/0034268) with the teachings of Miyanabe (US 6134211) to configure a signal processor where the fixed clock is asynchronous with respect to the bit clock from the PLL circuit, so, to prevent having multiple clocks with same period or phase.

Regarding claim 7, Miyanabe (US 2002/0034268) further discloses, an apparatus (Fig. 2, element S and [0073]) for reading a signal stored along a track (ST1, MT, ST2) on a storage medium (DK) comprising a signal processor (Fig. 2, element 6) as claimed in claim 4.

Regarding claim 5, Miyanabe (US 2002/0034268) in view of Miyanabe (US 6134211) and Audoin (US 5703845) discloses, the signal processor as claimed in claim 4.

Miyanabe (US 6134211) further discloses, wherein said bit clock has a bit clock frequency (Fig. 6, element SYC at logic levels 1 and 0 comprise bit clock signal. It is inherent that clock signals comprise clock frequencies) and said fixed clock has a fixed clock frequency that is substantially different from said bit clock frequency such that the ratio between said bit clock frequency and said fixed clock frequency is substantially different from one (Fig. 5, elements 10, 5a-c and col. 5, lines 52-55 discloses a clock signal supplied from the PLL circuit to the A/D converters. Fig. 6, element 400 and col. 3, line 66-col. 4, line 4 discloses fixed coefficient values representing fixed clock. It is inherent that fixed clocks comprise fixed clock frequency. Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to recognized that the fixed clock frequency differs from the bit clock frequency as they are both distinct from each other; as such, the ratio between them is different from one).

Regarding claim 8, Miyanabe (US 2002/0034268) further discloses, an apparatus (Fig. 2, element S and [0073]) for reading a signal stored along a track (ST1, MT, ST2) on a storage medium (DK) comprising a signal processor (Fig. 2, element 6) as claimed in claim 5.

Response to Arguments

3. Applicant's arguments, filed on March 24, 2008, with respect to claims1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHIBUIKE K. NWAKAMMA whose telephone number is (571)270-3458. The examiner can normally be reached on Mon-Thur and Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen can be reached on 5712727579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. K. N./
Examiner, Art Unit 2627

/Thang V. Tran/
Primary Examiner, Art Unit 2627